UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/069,200	02/22/2002	Edward Allen Hall	RCA 89762	1634

7590 06/18/2004

Joseph S Tripoli
Thomson multimedia Licensing
P O Box 5312
Princeton, NJ 08540

EXAMINER	
LE, DUY K	

ART UNIT	PAPER NUMBER
2685	3

DATE MAILED: 06/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/069,200	HALL ET AL.	
	Examiner	Art Unit	
	Duy K Le	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-24 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, 9-14, 17, 18, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Badger (U.S. Patent 5,678,211).

As to claim 1, Figure 1 in Badger shows a tuner (10) comprising:

a phase-locked loop circuit (28) (see Col. 2, lines 4-54);

a nonvolatile memory (42) that stores alignment data (see Col. 2, lines 4-54),

As to claim 2, Figure 1 in Badger shows the tuner of claim 1, wherein the alignment data can be utilized by the phase locked loop (see Col. 2, lines 27-38).

As to claim 3, Figure 1 in Badger shows the tuner of claim 1, wherein the nonvolatile memory is an EEPROM (see Col. 2, lines 48-54. The PROM 42 can be written via bus line 48 so it is functionally an EEPROM).

As to claim 4, Figure 1 in Badger shows the tuner of claim 1, wherein the tuner is used in a television receiver ("FIG. 1 shows a tuner section 10 of a television apparatus" (Col. 2, line 4)).

As to claim 5, Figure 1 in Badger shows the tuner of claim 4, wherein the tuner is coupled to a microprocessor (40), the microprocessor is contained in the television receiver (see Col. 2, lines 23-33).

As to claim 9, Figure 1 in Badger shows the tuner of claim 1, further comprising a D/A converter (32, 34, 36) (see Col. 2, lines 27-30).

As to claim 10, Figure 1 in Badger shows the tuner of claim 1, wherein the tuner further comprises an address decoder (40) (see Col. 2, lines 27-30).

As to claim 11, Figure 1 in Badger shows the tuner of claim 10, wherein the address decoder includes a 1 to 1 actual channel to alignment channel addressing scheme (see Col. 2, lines 48-54).

As to claim 12, Figure 1 in Badger shows the tuner of claim 10, wherein the address decoder includes a plurality to 1 actual channel to alignment channel addressing scheme (see Col. 3, lines 44-59).

As to claim 13, Figure 1 in Badger shows the tuner of claim 10, wherein the address decoder is implemented using software (see Col. 4, lines 45-49. It is inherent that the processor means to retrieve data from the memory can be implemented in software).

As to claim 14, Figure 1 in Badger shows the tuner of claim 10, wherein the address decoder is implemented using hardware (see Col. 2, lines 27-30 and Figure 1).

As to claim 17, Figure 1 in Badger shows a television control system for tuning a desired television signal, which comprises:

a radio frequency (RF) source (12) for receiving an RF signal associated with television channels (see Col. 2, lines 4-54);

a tuner module (10), coupled to said RF source, for selecting the desired television signal from said RF signal, said tuner module having a memory unit, wherein said memory unit contains alignment data for said tuner module (see Col. 2, lines 4-54); and

a microprocessor (40), coupled to said tuner module, for communicating a tuning command corresponding to the desired television signal to said tuner module (see Col. 2, lines 4-54).

As to claim 18, Figure 1 in Badger shows the television control system of claim 17 wherein said tuner module comprises:

a downconverter (24), coupled to said RF source, for selecting a RF signal corresponding to the desired television signal (see Col. 2, lines 12-15);

a phase locked loop (PLL) (28), coupled to said microprocessor and said downconverter, for receiving said tuning command and generating a frequency tone for output (see Col. 2, lines 11-15 and lines 31-36); and

an address decoder (40), coupled to said PLL and said memory unit, wherein said address decoder retrieves said alignment data from a memory location in said memory unit for the desired television signal (see Col. 2, lines 27-30).

As to claim 20, Figure 1 in Badger shows the television control system of claim 17 wherein said memory unit comprises an electrically erasable programmable read only memory (EEPROM) (see Col. 2, lines 48-54. The PROM 42 can be written via bus line 48 so it is functionally an EEPROM).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6, 8, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,678,211 to Badger in view of Bonneau et al. (U.S. Patent 4,510,623).

As to claim 6, Figure 1 in Badger shows the tuner of claim 1. However, it does not expressly disclose the phase locked loop circuit is a phase-locked loop integrated circuit. The Bonneau reference teaches the phase locked loop circuit is a phase-locked loop integrated circuit ("the description of the PLL 12 has been brief because such a device may be purchased as an off-the-shelf item, i.e., TD6306P, from Toshiba Corporation, and literature on the device is readily available" (Col. 4, lines 19-22)).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the tuner of Badger wherein the phase locked loop circuit is a phase-locked loop integrated circuit, as taught by Bonneau, in order to use an off-the-shelf device for PLL.

As to claim 8, Badger-Bonneau discloses the tuner of claim 6, wherein the re-writable memory (42) is coupled to, but not integrated in, the phase-locked loop integrated circuit (Badger; see Col. 2, lines 23-54).

As to claim 19, the Badger reference discloses the television control system of claim 17. However, it does not expressly disclose the microprocessor is coupled to the tuner module via an inter-integrated circuit bus. The Bonneau reference teaches the microprocessor is coupled to the tuner module via an inter-integrated circuit bus (see Col. 3, lines 18-24, Col. 4, lines 19-22, Col. 5, lines 2-4, and Figure 1. The PLL can be an IC and as part of a tuner, and the microprocessor can be another IC. Hence, the microprocessor is coupled to the tuner module via an inter-

integrated circuit bus ("the microprocessor 13 supplies data and load commands to the PLL 12 via the PLL data bus 127" (Col. 4, lines 10-12)).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Badger wherein the microprocessor is coupled to the tuner module via an inter-integrated circuit bus, as taught by Bonneau, in order to supply data and load commands to the PLL via the PLL data bus.

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,678,211 to Badger in view of Bonneau et al. (U.S. Patent 4,510,623) and further in view of Wu et al. (U.S. Patent 6,557,117).

As to claim 7, Badger-Bonneau discloses the tuner of claim 6. However, it does not disclose the re-writable memory is integrated in the phase locked loop integrated circuit. The Wu reference teaches the re-writable memory is integrated in the phase locked loop integrated circuit (see Col. 2, lines 55-65 and Figure 2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Badger-Bonneau wherein the re-writable memory is integrated in the phase locked loop integrated circuit, as taught by Wu, in order to test the PLL without external access.

6. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,678,211 to Badger in view of Mogi (U.S. Patent 4,326,220).

As to claim 15, Figure 1 in Badger shows a television receiver comprising:

a microprocessor (40) (see Col. 2, lines 23-33);

a first nonvolatile memory (42) coupled to the microprocessor (see Col. 2, lines 23-47);

a tuner coupled to the microprocessor, the tuner comprising:

a phase-locked loop circuit (28) coupled to the microprocessor (see Col. 2, lines 4-54).

However, it does not disclose a second non-volatile memory. The Mogi reference teaches a second non-volatile memory ("ROM 14" in Col. 2, lines 27-36).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the receiver of Badger wherein the tuner comprises a second non-volatile memory, as taught by Mogi, in order to store the frequency dividing ratio of programmable frequency divider in response to a channel to be received.

As to claim 16, Badger-Mogi discloses the television receiver of claim 15, wherein Mogi discloses the second nonvolatile memory is a ROM that can store alignment data. The Badger reference teaches the nonvolative memory can be EEPROM (see Col. 2, lines 48-54. The PROM 42 can be written via bus line 48 so it is functionally an EEPROM) in order to write data into the memory.

7. Claims 21, 22, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,678,211 to Badger in view of Hisada et al. (U.S. Patent 6,281,946).

As to claim 21, Figure 1 in Badger shows a television receiver for receiving a desired television signal, which comprises:

a radio frequency (RF) source (12) for receiving an RF signal associated with television channels (see Col. 2, lines 4-54);

a tuner module (10), coupled to said RF source, for generating an RF signal corresponding to the desired television signal, said tuner module having a memory unit, wherein said memory unit contains alignment data for said tuner module (see Col. 2, lines 4-54);

an intermediate frequency (IF) module (24), coupled to said tuner module, for converting said RF signal corresponding with the desired television signal to an IF signal (see Col. 2, lines 12-17).

However, it does not disclose a demodulation module, coupled to said IF module, for demodulation and display of the television information of the desired television signal. The Hisada reference teaches a demodulation module, coupled to said IF module, for demodulation and display of the television information of the desired television signal (see Col. 2, lines 20-35 and Figure 1).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the receiver of Badger to comprise a demodulation module, coupled to said IF module, for demodulation and display of the television information of the desired television signal, as taught by Hisada, in order to reproduce an image from the received video signal.

As to claim 22, Badger-Hisada discloses the television receiver of claim 21. The Badger reference further discloses said tuner module comprises:

a downconverter (24), coupled to said RF source, for selecting said RF signal corresponding to the desired television signal (see Col. 2, lines 12-15);

a phase locked loop (PLL) (28), coupled to said microprocessor and said downconverter, for generating a frequency tone for output (see Col. 2, lines 11-15 and lines 31-36); and

an address decoder (40), coupled to said PLL and said memory unit, wherein said address decoder retrieves said alignment data from a memory location in said memory unit for the desired television signal (see Col. 2, lines 27-30).

As to claim 24, Badger-Hisada discloses the television receiver of claim 21 wherein said memory unit comprises an electrically erasable programmable read only memory (EEPROM) (Badger; see Col. 2, lines 48-54. The PROM 42 can be written via bus line 48 so it is functionally an EEPROM).

8. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,678,211 to Badger in view of Hisada et al. (U.S. Patent 6,281,946) and further in view of Bonneau et al. (U.S. Patent 4,510,623).

As to claim 23, Badger-Hisada discloses the television receiver of claim 21. However, it does not expressly disclose the microprocessor is coupled to the tuner module via an inter-integrated circuit bus. The Bonneau reference teaches the microprocessor is coupled to the tuner module via an inter-integrated circuit bus (see Col. 3, lines 18-24, Col. 4, lines 19-22, Col. 5, lines 2-4, and Figure 1. The PLL can be an IC and as part of a tuner, and the microprocessor can be another IC. Hence, the microprocessor is coupled to the tuner module via an inter-integrated circuit bus ("the microprocessor 13 supplies data and load commands to the PLL 12 via the PLL data bus 127" (Col. 4, lines 10-12)).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the receiver of Badger-Hisada wherein the microprocessor is coupled to the tuner module via an inter-integrated circuit bus, as taught by Bonneau, in order to supply data and load commands to the PLL via the PLL data bus.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Kumamoto et al. (U.S. Patent 4,691,378) discloses tuner for television receiver.

b. Basile et al. (U.S. Patent 5,067,011) discloses method and apparatus for demodulating chrominance signals using a training signal in place of a color burst signal.

c. Couet (U.S. Patent 5,828,266) discloses apparatus and methods for setting up a tuning frequency of a PLL demodulator that compensates for dispersion and aging effects of an associated ceramic resonator frequency reference.

d. Brekelmans (U.S. Patent 6,151,488) discloses multi-tuner receiver for concurrent reception of mutually different signals.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duy K Le whose telephone number is 703-305-5660. The examiner can normally be reached on 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward F Urban can be reached on 703-305-4385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Duy Le
June 7, 2004

EDWARD F. URBAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600